CLAIMS

I claim:

1. In a logic emulation system, a method for transmitting a data packet between substantially asynchronous components, comprising:

providing a transmit clock signal of a predetermined frequency;

transmitting serially over a connection between said asynchronous systems, in accordance with said transmit clock signal, a framing sequence; and

subsequent to transmitting said framing sequence, transmitting said data packet serially over said connection;

wherein each bit in said framing sequence and said data packet is transmitted over two transmit clock periods.

2. In a logic emulation system, a method for receiving a data packet between asynchronous systems, comprising:

providing a receive clock signal of a predetermined frequency;

detecting a framing sequence transmitted serially over a connection between said asynchronous systems, in accordance with said receive clock signal; and

subsequent to receiving said framing sequence, receiving said data packet serially over said connection;

wherein each bit in said framing sequence and said data packet is received over two receive clock periods.

3. A method as in Claim 2, wherein said asynchronous systems comprise two portions of an emulation circuit implemented on different circuit boards housed in separate chassis.

4. A method as in Claim 2, wherein said asynchronous systems comprise a portion of an emulation circuit and a controller housed in a host computer.

5. A logic emulation system, comprising:

a circuit board including a plurality of programmable logic devices, said circuit board implementing an emulation circuit and a transmitter circuit, said circuit board receiving a clock signal of a predetermined frequency;

a controller coupled to a host computer, said controller having a receiver circuit and also receiving a clock signal of said predetermined frequency; and

a connection between said transmitter circuit and said receiver circuit, wherein each bit of data transmitted over said connection has a duration of two or more periods of said clock signal received at said circuit board.

6. An emulation circuit as in Claim 5, wherein said clock signal received at said circuit board and said clock signal received at said controller are provided by a common source.

7. An emulation circuit as in Claim 5, wherein said clock signal received at said circuit board and said clock signal received at said controller are generated independently.

8. An emulation circuit as in Claim 5, wherein said clock signal has the frequency of a virtual clock signal.

9. An emulation circuit as in Claim 5, wherein said clock signal has twice the frequency of a virtual clock signal.

10. An emulation circuit as in Claim 9, further comprising a phase-locked loop circuit for generating said clock signal from a virtual clock signal.

11. An emulation system, comprising:

a first circuit board including a plurality of programmable logic devices, said circuit board implementing an emulation circuit and a transmitter circuit, said circuit board receiving a clock signal of a predetermined frequency;

a second circuit board, said second circuit board having a receiver circuit and also receiving a clock signal of said predetermined frequency; and

a connection between said transmitter circuit and said receiver circuit, wherein each bit of data transmitted over said connection has a duration of two or more periods of said clock signal received at said first circuit board.

12. An emulation circuit as in Claim 11, wherein said clock signal received at said first circuit board and said clock signal received at said second circuit board are provided by a common source.

13. An emulation circuit as in Claim 11, wherein said clock signal received at said first circuit board and said clock signal received at said second circuit board are generated independently.

14. An emulation circuit as in Claim 11, wherein said clock signal has the frequency of a virtual clock signal.

15. An emulation circuit as in Claim 11, wherein said clock signal has twice the frequency of a virtual clock signal.

16. An emulation circuit as in Claim 15, further comprising a phase-locked loop circuit configured on said first circuit board for generating said clock signal from a virtual clock signal.